



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,245	08/29/2001	Tongbi Jiang	4241.1US (99-0408.1)	8370
24247	7590	03/25/2005	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			IM, JUNGHWAM	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EIV

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	09/942,245	JIANG, TONGBI	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 07 January 2005.
- 2a) This action is FINAL.                                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-16, 19-24, 26-41 and 44-49 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-16, 19-24, 26-41 and 44-49 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 7, 2005 has been entered.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-16, 19-24, 26-41 and 44-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (US 5,864,178), hereinafter Yamada in view of Hoge et al. (US 4,388,132), hereinafter Hoge.

Regarding claim 1, Fig. 54 of Yamada shows a semiconductor assembly comprising: a semiconductor device (or a die; 201) having an active surface having a plurality of bond pads (224);

a wetting agent layer (207, 208; a polymer layer excellent in wettability ; col. 54, lines 34-36) provided on the active surface of said semiconductor device (207).

Fig. 54 of Yamada shows the most aspect of the instant invention except a wetting agent layer "comprising a layer of solely silane-based material with undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material." Fig. 6B of Hoge shows a semiconductor device comprising a coupling agent layer (60; a wetting agent layer) of solely silane-based material (col. 5, lines 1-5) undergoing no substantial degradation thereof during one of a solder reflow process and a curing process for a material (col. 1, lines 49-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Hoge for the wetting agent layer of Yamada in order to have to the wetting agent layer comprised of a layer of solely silane-based material to promote the adhesion through utilizing a coupling material well known in the industry.

Regarding claims 2-4, Fig. 6B of Hoge discloses a wetting agent layer (60; a coupling agent layer) include at least one layer of ethyltrimethoxysilane (col. 5, lines 1-5).

Regarding claim 5, Yamada discloses the wetting agent layer reduces surface tension of the active surface throughout the specification especially in col. 20, lines 34-65. Furthermore, it is noted that the coupling layer of Hoge is comprised of the identical material to the one in the instant invention, therefore the silane-based layer also having surface tension of the active surface reduced.

Regarding claim 6, Fig.54 of Yamada shows a semiconductor assembly comprising:  
a semiconductor device (or a die; 201) having an active surface;

a substrate (202) having an upper surface;  
a semiconductor device (or a die; 201) having an active surface having a plurality of bond pads (224);  
a wetting agent layer (207, 208; a polymer layer excellent in wettability ; col. 54, lines 34-36) provided on the active surface of said semiconductor device (207).

Fig. 54 of Yamada shows the most aspect of the instant invention except a wetting agent layer “comprising a layer of solely silane-based material with undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material.” Fig. 6B of Hoge shows a semiconductor device comprising a coupling agent layer (60; a wetting agent layer) of solely silane-based material (col. 5, lines 1-5) undergoing no substantial degradation thereof during one of a solder reflow process and a curing process for a material (col. 1, lines 49-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Hoge for the wetting agent layer of Yamada in order to have the wetting agent layer comprised of a layer of solely silane-based material to promote the adhesion through utilizing a coupling material well known in the industry.

Regarding claims 7-9, Fig. 6B of Hoge discloses a wetting agent layer (60; a coupling agent layer) include at least one layer of ethyltrimethoxysilane (col. 5, lines 1-5).

Regarding claim 10, Fig. 54 of Yamada shows a semiconductor assembly comprising:  
a semiconductor device (or a die; 201) having an active surface;  
a substrate (202) having an upper surface;

a wetting agent layer (207, 208; a polymer layer excellent in wettability ; col. 54, lines 34-36) provided on the active surface of said semiconductor device (207).

an underfill material (encapsulation resin; col. 56, lines 20-26) to fill the gap between said substrate and said semiconductor device (or between the substrate and the wetting agent layer).

Fig. 54 of Yamada shows the most aspect of the instant invention except a wetting agent layer “comprising a layer of solely silane-based material with undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material.” Fig. 6B of Hoge shows a semiconductor device comprising a coupling agent layer (60; a wetting agent layer) of solely silane-based material (col. 5, lines 1-5) undergoing no substantial degradation thereof during one of a solder reflow process and a curing process for a material (col. 1, lines 49-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Hoge for the wetting agent layer of Yamada in order to have to the wetting agent layer comprised of a layer of solely silane-based material to promote the adhesion through utilizing a coupling material well known in the industry.

Regarding claims 11-13, Fig. 6B of Hoge discloses a wetting agent layer (60; a coupling agent layer) include at least one layer of ethyltrimethoxysilane (col. 5, lines 1-5).

Regarding claim 14, Fig. 54 of Yamada shows a semiconductor assembly comprising: a semiconductor device (or a die; 201) having an active surface having a plurality of bond pads (224);

a substrate (202; a circuit board) having an upper surface having a plurality of circuits thereon;

a plurality of bumps (203) connecting said plurality of bond pads on said active surface of said semiconductor device to said plurality of circuits on said upper surface of said substrate;

an underfill material (encapsulation resin; col. 56, lines 20-26) to fill the gap between said substrate and said semiconductor device (or between the substrate and the wetting agent layer);

a wetting agent layer (207, 208; a polymer layer excellent in wettability ; col. 54, lines 34-36) provided on the active surface of said semiconductor device (207).

Fig. 54 of Yamada shows the most aspect of the instant invention except a wetting agent layer “comprising a layer of solely silane-based material with undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material.”

Fig. 6B of Hoge shows a semiconductor device comprising a coupling agent layer (60; a wetting agent layer) of solely silane-based material (col. 5, lines 1-5) undergoing no substantial degradation thereof during one of a solder reflow process and a curing process for a material (col. 1, lines 49-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Hoge for the wetting agent layer of Yamada in order to have the wetting agent layer comprised of a layer of solely silane-based material to promote the adhesion through utilizing a coupling material well known in the industry.

Regarding claim 15 and 19, Fig. 6B of Hoge discloses a wetting agent layer (60; a coupling agent layer) include at least one layer of ethyltrimethoxysilane (col. 5, lines 1-5).

Regarding claim 16, Fig.54 of Yamada shows an additional wetting layer on the upper surface of the substrate (208; col. 56, lines 22-63 and col. 17, lines 53-59).

Regarding claim 20, Fig.54 of Yamada shows a semiconductor assembly comprising:  
a semiconductor device (or a die; 201) having an active surface;  
a substrate (202) having an upper surface;  
an underfill material (encapsulation resin; col. 56, lines 20-26) to fill the gap between said substrate and said semiconductor device (or between the substrate and the wetting agent layer).

a wetting agent layer (207, 208; a polymer layer excellent in wettability ; col. 54, lines 34-36) provided on the active surface of said semiconductor device (207).

Fig. 54 of Yamada shows the most aspect of the instant invention except a wetting agent layer “comprising a layer of solely silane-based material with undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material.”

Fig. 6B of Hoge shows a semiconductor device comprising a coupling agent layer (60; a wetting agent layer) of solely silane-based material (col. 5, lines 1-5) undergoing no substantial degradation thereof during one of a solder reflow process and a curing process for a material (col. 1, lines 49-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Hoge for the wetting agent layer of Yamada in order to have to the wetting agent layer comprised of a layer of solely silane-based material to promote the adhesion through utilizing a coupling material well known in the industry.

Regarding claim 21 and 22, Fig. 6B of Hoge discloses a wetting agent layer (60; a coupling agent layer) include at least one layer of ethyltrimethoxysilane (col. 5, lines 1-5).

Regarding claim 23, Fig. 54 of Yamada shows a semiconductor assembly comprising: a semiconductor device (or a die; 201) having an active surface having a plurality of bond pads (224);

a substrate (202; a circuit board) having an upper surface having a plurality of circuits thereon;

a plurality of bumps (203) connecting said plurality of bond pads on said active surface of said semiconductor device to said plurality of circuits on said upper surface of said substrate;

an underfill material (encapsulation resin; col. 56, lines 20-26) to fill the gap between said substrate and said semiconductor device (or between the substrate and the wetting agent layer).

a wetting agent layer (207, 208; a polymer layer excellent in wettability ; col. 54, lines 34-36) provided on the active surface of said semiconductor device (207).

Fig. 54 of Yamada shows the most aspect of the instant invention except a wetting agent layer “comprising a layer of solely silane-based material with undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material.”

Fig. 6B of Hoge shows a semiconductor device comprising a coupling agent layer (60; a wetting agent layer) of solely silane-based material (col. 5, lines 1-5) undergoing no substantial degradation thereof during one of a solder reflow process and a curing process for a material (col. 1, lines 49-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Hoge for the wetting agent layer of Yamada in order to have to the wetting agent layer comprised of a layer of solely silane-based material to promote the adhesion through utilizing a coupling material well known in the industry.

Regarding claim 24, Fig.54 of Yamada shows the underfill material substantially fills the gap between the semiconductor and the substrate.

Regarding claim 26, Fig.54 of Yamada shows a semiconductor die comprising:  
a semiconductor device (or a die; 201) having an active surface having a plurality of bond pads (224);  
a substrate (202; a circuit board) having an upper surface;  
a wetting agent layer (207, 208; a polymer layer excellent in wettability ; col. 54, lines 34-36) provided on the active surface of said semiconductor device (207).

Fig. 54 of Yamada shows the most aspect of the instant invention except a wetting agent layer "comprising a layer of solely silane-based material with undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material." Fig. 6B of Hoge shows a semiconductor device comprising a coupling agent layer (60; a wetting agent layer) of solely silane-based material (col. 5, lines 1-5) undergoing no substantial degradation thereof during one of a solder reflow process and a curing process for a material (col. 1, lines 49-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Hoge for the wetting agent layer of Yamada in order to have to the

wetting agent layer comprised of a layer of solely silane-based material to promote the adhesion through utilizing a coupling material well known in the industry.

Regarding claims 27-29, Fig. 6B of Hoge discloses a wetting agent layer (60; a coupling agent layer) include at least one layer of ethyltrimethoxysilane (col. 5, lines 1-5).

Regarding claim 30, Yamada discloses the wetting agent layer reduces surface tension of the active surface throughout the specification especially in col. 20, lines 34-65. Furthermore, it is noted that the coupling layer of Hoge is comprised of the identical material to the one in the instant invention, therefore the silane-based layer also having surface tension of the active surface reduced.

Regarding claim 31, Fig. 54 of Yamada shows a semiconductor die comprising:  
a semiconductor device (or a die; 201) having an active surface having a plurality of bond pads (224);  
a substrate (202; a circuit board) having an upper surface;  
a wetting agent layer (207, 208; a polymer layer excellent in wettability ; col. 54, lines 34-36), said wetting layer having a thickness of a monolayer provided on the active surface of said semiconductor device/die (207).

Fig. 54 of Yamada shows the most aspect of the instant invention except a wetting agent layer “comprising a layer of solely silane-based material with undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material.”

Fig. 6B of Hoge shows a semiconductor device comprising a coupling agent layer (60; a wetting agent layer) of solely silane-based material (col. 5, lines 1-5) undergoing no substantial

degradation thereof during one of a solder reflow process and a curing process for a material (col. 1, lines 49-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Hoge for the wetting agent layer of Yamada in order to have to the wetting agent layer comprised of a layer of solely silane-based material to promote the adhesion through utilizing a coupling material well known in the industry.

Regarding claims 32-34, Fig. 6B of Hoge discloses a wetting agent layer (60; a coupling agent layer) include at least one layer of ethyltrimethoxysilane (col. 5, lines 1-5).

Regarding claim 35, Fig. 54 of Yamada shows a semiconductor die comprising: a semiconductor device (or a die; 201) having an active surface having a plurality of bond pads (224);

a substrate (202; a circuit board) having an upper surface; a wetting agent layer (207, 208; a polymer layer excellent in wettability ; col. 54, lines 34-36 located on the active surface of said semiconductor device/die (207).

Fig. 54 of Yamada shows the most aspect of the instant invention except a wetting agent layer “comprising a layer of solely silane-based material with undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material.”

Fig. 6B of Hoge shows a semiconductor device comprising a coupling agent layer (60; a wetting agent layer) of solely silane-based material (col. 5, lines 1-5) undergoing no substantial degradation thereof during one of a solder reflow process and a curing process for a material (col. 1, lines 49-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Hoge for the wetting agent layer of Yamada in order to have to the wetting agent layer comprised of a layer of solely silane-based material to promote the adhesion through utilizing a coupling material well known in the industry.

Regarding claims 36-38, Fig. 6B of Hoge discloses a wetting agent layer (60; a coupling agent layer) include at least one layer of ethyltrimethoxysilane (col. 5, lines 1-5).

Regarding claim 39, Fig. 54 of Yamada shows a semiconductor die comprising:  
a semiconductor device (or a die; 201) having an active surface having a plurality of bond pads (224);

a substrate (202; a wiring circuit board) having an upper surface having a plurality of circuits;

a plurality of bumps (203) connecting said plurality of bond pads on said active surface of said semiconductor device to said plurality of circuits on said upper surface of said substrate;

said plurality of bumps forming a gap between said semiconductor device and said substrate;

an underfill material (encapsulation resin; col. 56, lines 20-26) to fill the gap between said substrate and said semiconductor device (or between the substrate and the wetting agent layer);

a wetting agent layer (207, 208; a polymer layer excellent in wettability ; col. 54, lines 34-36) provided on the active surface of said semiconductor device (207) and on a upper surface of substrate (208; col. 56, lines 22-63 and col. 17, lines 53-59).

Fig. 54 of Yamada shows the most aspect of the instant invention except a wetting agent layer “comprising a layer of solely silane-based material with undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material.” Fig. 6B of Hoge shows a semiconductor device comprising a coupling agent layer (60; a wetting agent layer) of solely silane-based material (col. 5, lines 1-5) undergoing no substantial degradation thereof during one of a solder reflow process and a curing process for a material (col. 1, lines 49-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Hoge for the wetting agent layer of Yamada in order to have to the wetting agent layer comprised of a layer of solely silane-based material to promote the adhesion through utilizing a coupling material well known in the industry.

Regarding claims 40 and 44, Fig. 6B of Hoge discloses a wetting agent layer (60; a coupling agent layer) include at least one layer of ethyltrimethoxysilane (col. 5, lines 1-5).

Regarding claim 41, Fig. 54 of Yamada shows the underfill material substantially fills the gap between the semiconductor and the substrate.

Regarding claim 45, Fig. 54 of Yamada shows a semiconductor die comprising:  
a semiconductor device (or a die; 201) having an active surface;  
a substrate (202; a wiring circuit board) having an upper surface;  
an underfill material (encapsulation resin; col. 56, lines 20-26) to fill the gap between said substrate and said semiconductor device (or between the substrate and the wetting agent layer);

a wetting agent layer (207, 208; a polymer layer excellent in wettability ; col. 54, lines 34-36) provided on the active surface of said semiconductor device (207) and on a upper surface of substrate (208; col. 56, lines 22-63 and col. 17, lines 53-59).

Fig. 54 of Yamada shows the most aspect of the instant invention except a wetting agent layer “comprising a layer of solely silane-based material with undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material.” Fig. 6B of Hoge shows a semiconductor device comprising a coupling agent layer (60; a wetting agent layer) of solely silane-based material (col. 5, lines 1-5) undergoing no substantial degradation thereof during one of a solder reflow process and a curing process for a material (col. 1, lines 49-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Hoge for the wetting agent layer of Yamada in order to have to the wetting agent layer comprised of a layer of solely silane-based material to promote the adhesion through utilizing a coupling material well known in the industry.

Regarding claims 46-47, Fig. 6B of Hoge discloses a wetting agent layer (60; a coupling agent layer) include at least one layer of ethyltrimethoxysilane (col. 5, lines 1-5).

Regarding claim 48, Fig. 54 of Yamada shows a semiconductor die comprising:  
a semiconductor device (or a die; 201) having an active surface having a plurality of bond pads (224);  
a substrate (202; a wiring circuit board) having an upper surface having a plurality of circuits;

a plurality of bumps (203) connecting said plurality of bond pads on said active surface of said semiconductor device to said plurality of circuits on said upper surface of said substrate;

said plurality of bumps forming a gap between said semiconductor device and said substrate;

an underfill material (encapsulation resin; col. 56, lines 20-26) to fill the gap between said substrate and said semiconductor device (or between the substrate and the wetting agent layer);

a wetting agent layer (207, 208; a polymer layer excellent in wettability ; col. 54, lines 34-36) provided on the active surface of said semiconductor device (207) and on a upper surface of substrate (208; col. 56, lines 22-63 and col. 17, lines 53-59).

Fig. 54 of Yamada shows the most aspect of the instant invention except a wetting agent layer “comprising a layer of solely silane-based material with undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material.”

Fig. 6B of Hoge shows a semiconductor device comprising a coupling agent layer (60; a wetting agent layer) of solely silane-based material (col. 5, lines 1-5) undergoing no substantial degradation thereof during one of a solder reflow process and a curing process for a material (col. 1, lines 49-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Hoge for the wetting agent layer of Yamada in order to have to the wetting agent layer comprised of a layer of solely silane-based material to promote the adhesion through utilizing a coupling material well known in the industry.

Regarding claim 49, Fig.54 of Yamada shows the underfill material substantially fills the gap between the semiconductor and the substrate.

***Response to Arguments***

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

*[Handwritten signature of Eddie C Lee]*  
Eddie Lee  
SPT TC 2800